**Digital Keypad Access Lock System**

**Project Proposal**

**University of UTAH Asia Campus**  
**Department of Electrical and Computer Engineering**  
**Course:** Digital System Design (ECE‑3700)

**Project Title**

**Digital Keypad Access Lock**

**Team Members**

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**Supervisor / Instructor:** Muhammad Raheel Bhutta

**Project Goal**

Design and implement a digital keypad access lock on an FPGA that accepts a 4-bits of password through a keypad and produces visual signal by turning LEDs on or off when the correct sequence is entered. The design emphasizes reliable keypad input handling (debouncing), basic user interaction, and password encryption.

**Learning Outcomes**

By completing this project we will learn to:

* Design and implement finite state machines to track sequences of key presses.
* Interface a matrix keypad with an FPGA.
* Control LEDs to indicate **Locked** and **Unlocked** states.
* Store and verify a password; optionally explore lightweight encryption (XOR) for stored credentials.
* Practice teamwork, documentation, and presentation skills.

**Project Scope (Baseline)**

* Implement a 3×4 or 4×4 keypad interface with FPGA-based debouncing.
* Accept a password input from the user through the keypad. (Ex: 1125#)
* # key tells the FSM input is complete, so it moves to the CHECK state.
* Apply a simple encryption method (XOR encryption with a key) to the user-entered password.
* Compare the encrypted user input with the encrypted default password stored in Verilog.
  + If they match → system unlocks (Green LED ON).
  + If they don’t match → system remains locked (Red LED ON).
* Target platform: FPGA development board (Model: 10M50DAF484C7G).

**Optional extensions:**

* Use non-volatile User Flash Memory (UFM) (~1.6 Mbit) to store the password, ensuring it remains saved after power-off.
* Integrate a 7-segment or character LCD display to show entered digits or system status messages.
* Implement full password storage and retrieval using non-volatile memory for persistent operation.

**Hardware / Tools (proposed)**

* FPGA development board
* Matrix keypad (3×4 or 4×4)
* Two LEDs for locked/unlocked indication
* Wires/jumpers to connect LEDs and keypad
* Development tools: Quartus/ModelSim, Verilog/VHDL

**Work Distribution**

The workload will be distributed equally, with both members contributing to the project using a parallel editing approach. Each member will take turns working on the FPGA hardware side and writing code in Verilog.